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A 1 To 40 GHz MESFET HYBRID DISTRIBUTED AMPLIFIER

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ABSTRACT

A 1 - 40 GHz hybrid amplifier with 10 dB minimum gain up to 40 GHz and using 0.3 micron MESFETs is presented. Gain ripple is +/- 1 dB in the 1 to 26.5 GHz range. Maximum noise figure is 7.5 dB in the 2 - 18 GHz range, and output power at one dB gain compression is 11 dBm.

The circuit includes a 1-40 GHz biasing system. Device S parameters were measured in the 1 20 GHz band. and static measurements were used to derive an equivalent circuit of the FET leading to very good agreement between simulations and measurements up to 40 GHz.

INTRODUCTION

The need for electronic warfare receivers with always widening frequency range has recently [illegible] state-of-the art realizations of 2-40 GHz amplifiers (1), (2), (3), (4). All of these reported devices are MMICs, and the most recent ones are based on HEMT material.

But the cost and reliability of HEMT millimetric devices, as well as the problems involved with MMIC integration of high value capacitors required in a 1-40 GHz passive biasing system, led us to choose a hybrid MESFET based technology to realize a directly integrable 1-40 GHz amplifier.

AMPLIFIER DESIGN

Distributed amplifiers have demonstrated ultra wide band performance for long. But the design of a 1-40 GHz amplifier rises two major problems :

Primerly, the gain performance in the higher frequency range, which is mainly dependent on the optimal number of FET cells and of their elementary gate width.

Then the lower-band gain, which is directly linked with the implementation of a high-performance biasing system, providing both gate and drain lines with the required termination and bias input.

Another point to mention is that simulation, to be effective at higher frequency, must take into account every parasitic element introduced by the technology, such as open-end effects which turn out to be under estimated in conventional CAD softwares for frequencies above 20 GHz (5). This also requires a reproductible, long experienced technology, and a comprehensive simulation of tolerances involved with the manufacturing.

The overall electric circuit for one distributed stage is presented in fig. 1 and incorporates six 0.3 x 64 microns FETs.

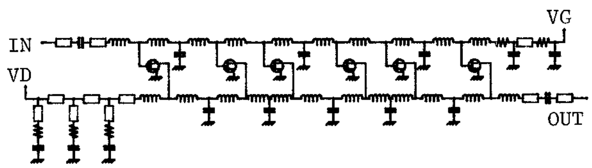

Fig. 1 : Schematic diagram of one 1-40 GHz distributed amplifier stage.

The gate-line termination consists of a simple resistance and a bypass capacitor. A series resistor was added to avoid unstability problems. The drain-line termination, designed to carry drain current towards the FETs, is more complex : it consists of three series R-C cells, shunting a simple transmission line. This passive network achieves 1-40 GHz performance, with no added power consumption nor yield or reliability degradation.

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The circuit has been implemented on 254 microns thick alumina, all bonding wires being 17 microns gold wires. A photograph of the two stages amplifier circuit is shown in fig. 2 with a close-up on the active devices in fig. 3.

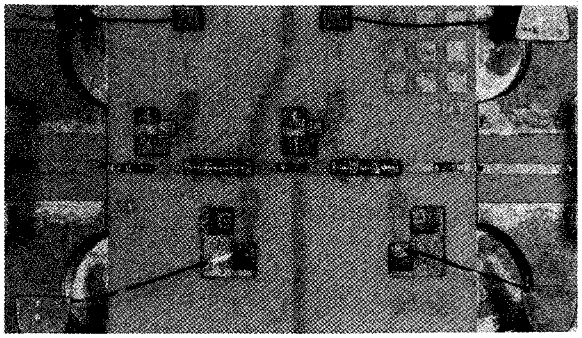


Fig. 2 : Photograph of the realized two-stage amplifier.

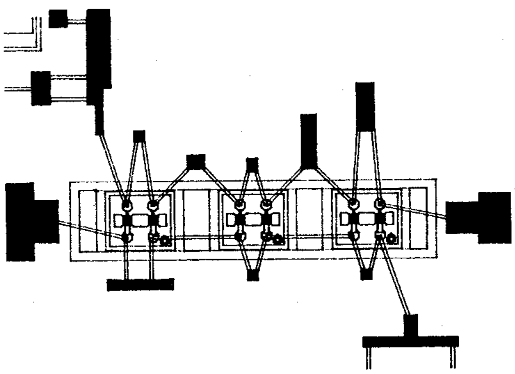
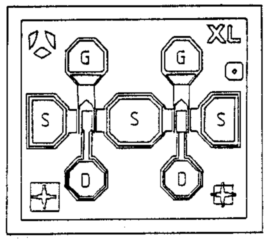


Fig. 3 : Close-up on the active devices.

DEVICE

The device used in this amplifier is a commercially available THOMSON-CSF MESFET. The EC1840 is composed of two independant cells, each cell with two 32 microns gate fingers. The gate length is 0.3 micron. The geometry of this device is presented in fig. 4.



400 x 300 microns

Fig. 4 : Geometry of the THOMSON-CSF EC 1840.

The typical RF performance measured on one 64 um cell are :

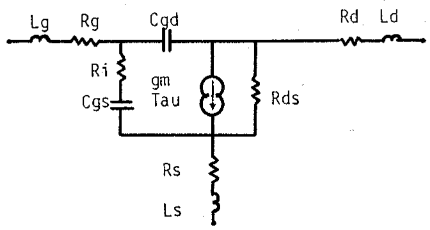
. MAG : 10 dB at 40 GHz.

. NF : 1.9 dB at 18 GHz with an associated gain of 11 dB.

Static and low frequency S parameter measurements were performed at various biasing points such as zero current, positive drain bias, to extract extrinsec elements of the equivalent circuit. This was done following the technique described in (6) and (7).

S parameters were measured from 1 to 20 GHz and the intrinsec equivalent circuit was derived.

The equivalent circuit for one 64 microns cell is given in fig. 5 for nominal bias point Vds = 3 V, Idss = 13 mA.



Lg	0.12 nH	Ri	12 Ω
Ld	0.2 nH	Cgs	47 fF
Ls	0.08 nH	Cgd	7 fF
Rg	4 Ω	Rds	520 Ω
Rd	7 Ω	gm	21 mS
Rs	7 Ω	Tau	1.6 ps

Fig. 5 : Equivalent circuit of one EC 1840 cell.

The very low value of the input capacitance Cgs allows the use of fairly high inductances, thus enabling the implementation of the amplifier using conventional bonding methods without degrading the high cut-off frequency of the artificial gate transmission line.

The high frequency potential performance of this device is clearly shown by the high gm/Cgs ratio (457mS/pF). A transconductance of 300 mS/mm is typically achieved at Idss, and the typical pinchoff voltage is 1.5 V.

A computer simulation of the complete two-stage amplifier using this equivalent circuit is compared with actual performance in fig. 6.

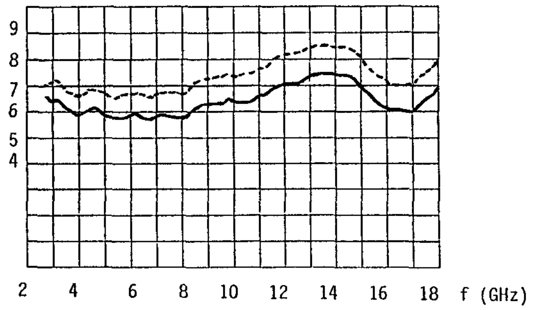


Fig. 7 : 2-18 GHz Noise Figure of the two stage amplifier
---- : Vds = 3 V, Vgs = 0 V, Ids = 170 mA
—— : Vds = 3 V, Vgs = - 0.2 V, Ids = 130 mA

AMPLIFIER'S MEASURED PERFORMANCE

Practical realization has led to a very good fit between predicted and measured performance :

As shown in fig. 6, an average gain of 15 dB is achieved, with a ripple of +/-1 dB in the 1-26.5 GHz range.

The minimum gain is 10 dB at 40 GHz.

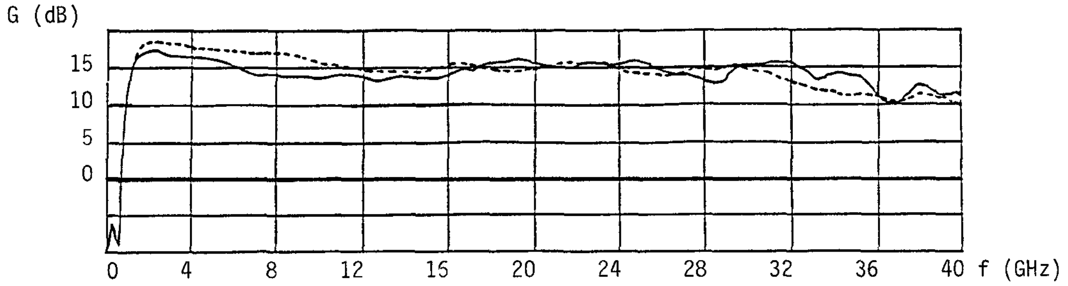


Fig. 6 : Simulated (---) and measured (-) performance of the two stage 1-40 GHz amplifier.

Noise figure measurements have been performed in the 2-18 GHz band. A maximum of 7.5 dB was obtained for two stages and 15 dB average gain at minimum noise bias (Vds = 3 V and Vgs = - 0.2 V). Noise figure has also been measured for maximum gain bias and reaches 8.5 dB in the same frequency range. Actual performance is presented in fig. 7 for both bias points.

Gain variation versus temperature has been measured in the - 40/+80oC range and is about the same as for conventional 0.5 micron FET devices, i.e. 0.018 dB/oC per stage, leading to a +/-2 dB gain variation in the whole temperature range.

Output power, measured at 6 GHz, shows a 1 dB compression point at 11 dBm, and a satured output power of 14 dBm. The saturation performance is presented in fig. 8, together with second harmonic level. It can be mentioned that this output power is achieved with only 384 microns of total gatewidth for the output stage, leading to a 34 mW/mm performance (at 1 dB compression point), which is higher than previously published 2-40 GHz MESFET based amplifiers.

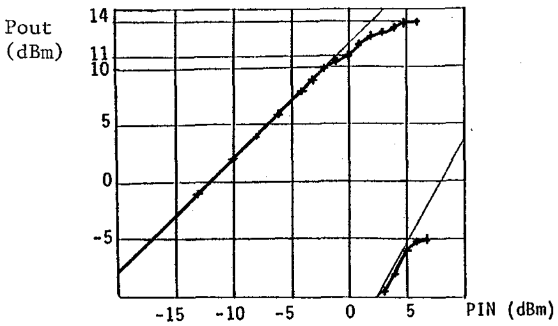


Fig. 8 : Output power measured at F = 6 GHz, with second harmonic level. Vds = 3 V, VGS = - 0,2 V.

CONCLUSION

This paper has described a directly integrable, 1-40 GHz hybrid amplifier using 0.3 micron MESFETs.

Results show excellent performance and very good agreement between simulation and actual measurements.

We demonstrated 1-40 GHz amplifier with 15 dB average gain and +/-1 dB ripple in the 1 to 26.5 GHz range, with a minimum of 10 dB at 40 GHz.

Noise figure is better than 7 dB in the 2 to 18 GHz range, and 1 dB gain compression point is 11 dBm.

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